SGS-THOMSON MICROELECTRONICS

M54HC595
M74HC595

8 BIT SHIFT REGISTER WITH OUTPUT LATCHES (3 STATE)

- HIGH SPEED
  f_{MAX} = 55 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS FOR QA TO QH
  10 LSTTL LOADS FOR QH'
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.) FOR QA TO QH
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.) FOR QH'
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH LSTTL 54/74LS595

B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :
M54HC595F1R   M74HC595M1R
M74HC595B1R   M74HC595C1R
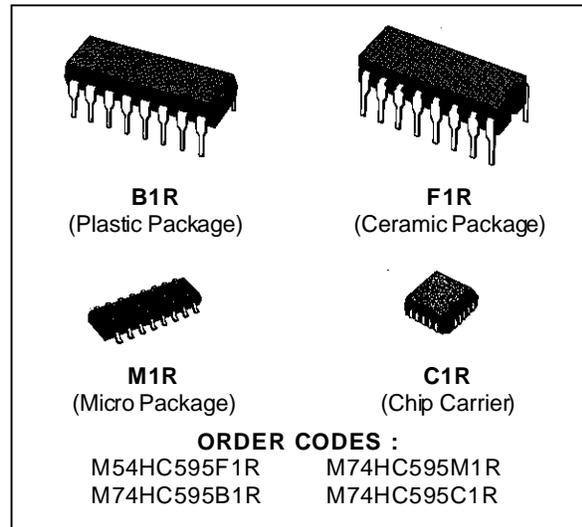
DESCRIPTION

The M54/74HC595 is a high speed CMOS 8-BIT SHIFT REGISTERS/OUTPUT LATCHES (3-STATE) fabricated in silicon C^{2}MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register.

The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)

QB 1	16 VCC
QC 2	15 QA
QD 3	14 SI
QE 4	13 $\overline{G}$
QF 5	12 RCK
QG 6	11 SCK
QH 7	10 $\overline{SCLR}$
GND 8	9 QH'

S-7086/1
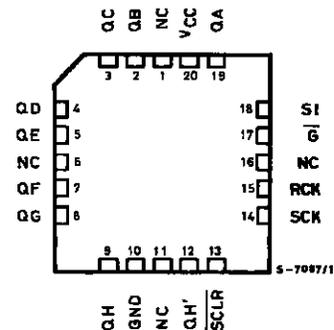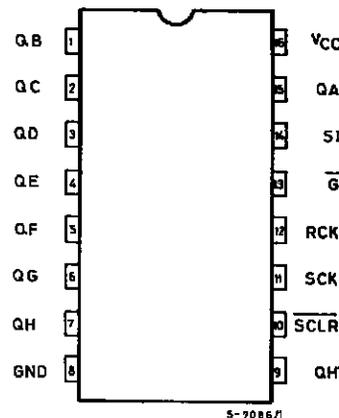
NC =
No Internal
Connection

INPUT AND OUTPUT EQUIVALENT CIRCUIT
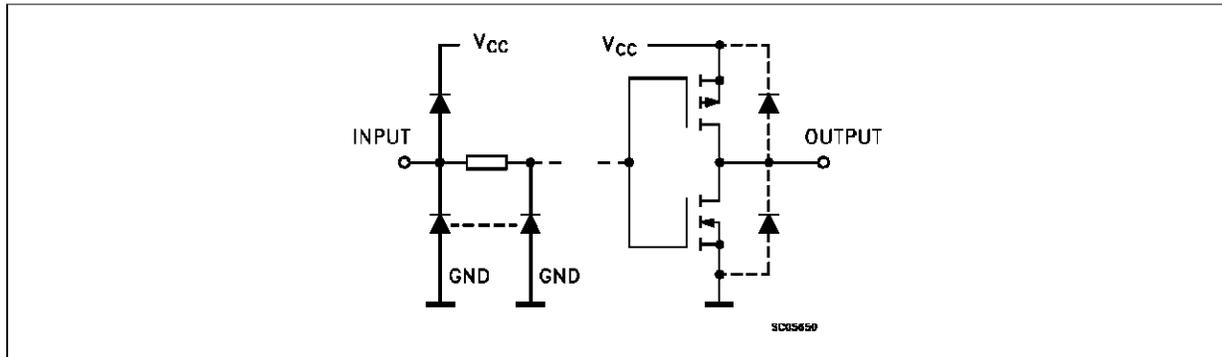
TRUTH TABLE

INPUTS					OUTPUT
SI	SCK	$\overline{\text{SCLR}}$	RCK	$\overline{\text{G}}$	
X	X	X	X	H	QA THRU QH OUTPUTS DISABLE
X	X	X	X	L	QA THRU QH OUTPUTS ENABLE
X	X	L	X	X	SHIFT REGISTER IS CLEARED
L	⌐	H	X	X	FIRST STAGE OF S.R. BECOMES "L" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
H	⌐	H	X	X	FIRST STAGE OF S.R. BECOMES "H" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
X	⌐L	H	X	X	STATE OF S.R IS NOT CHANGED
X	X	X	⌐	X	S.R. DATA IS STORED INTO STORAGE REGISTER
X	X	X	⌐L	X	STORAGE REGISTER STATE IS NOT CHANGED

X: DON'T CARE

LOGIC DIAGRAM

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MICROELECTRONICS

LOGIC DIAGRAM

S-10031
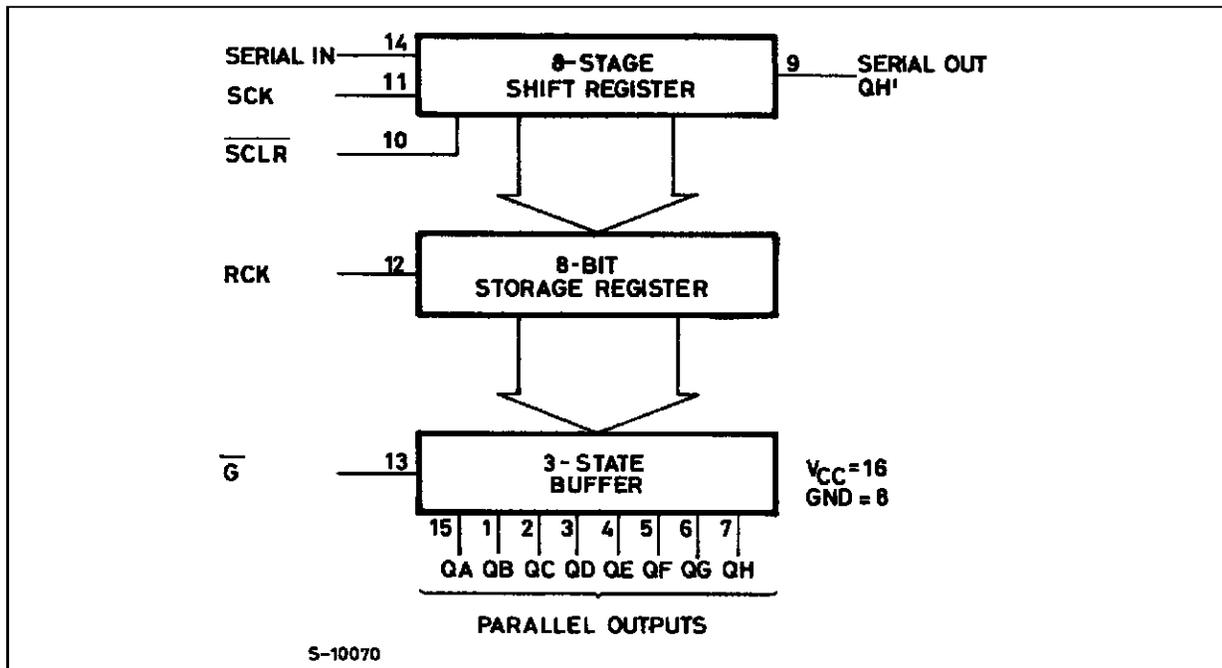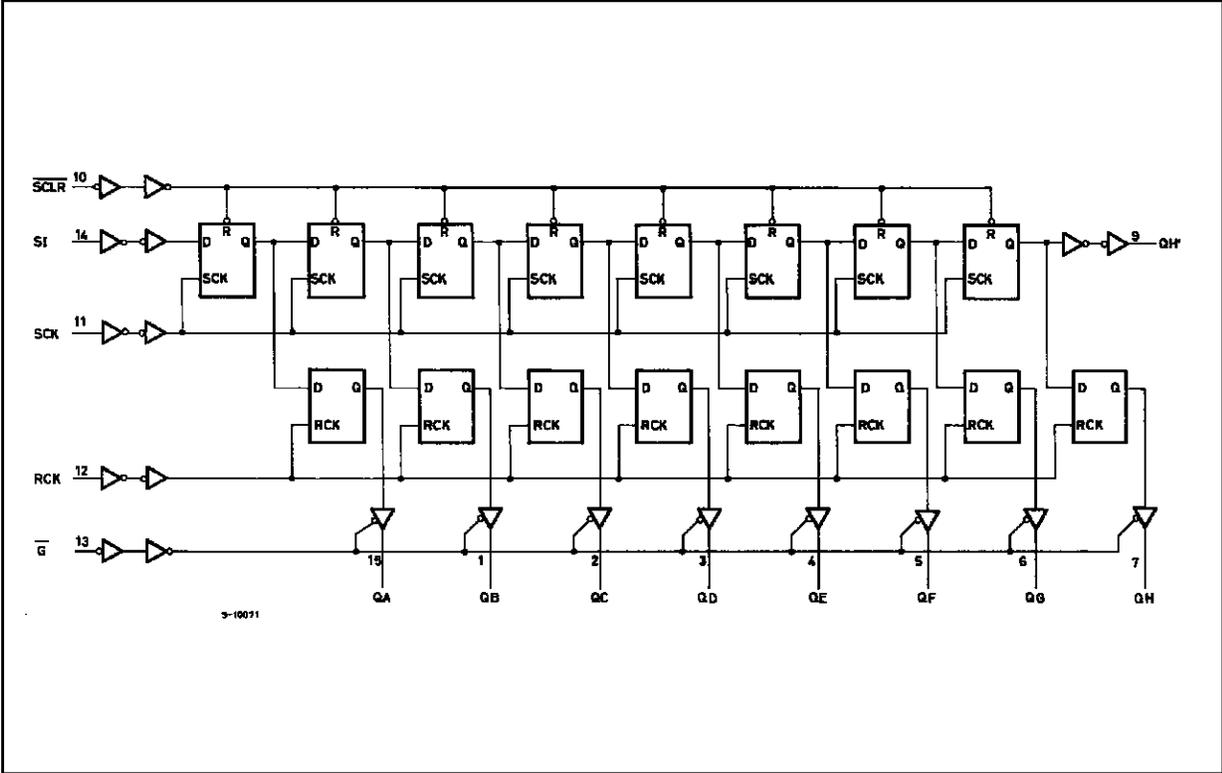
TIMING CHART

(NOTE) ⊠⊠ : HIGH IMPEDANCE

S-10072

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