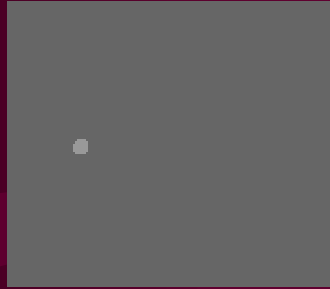
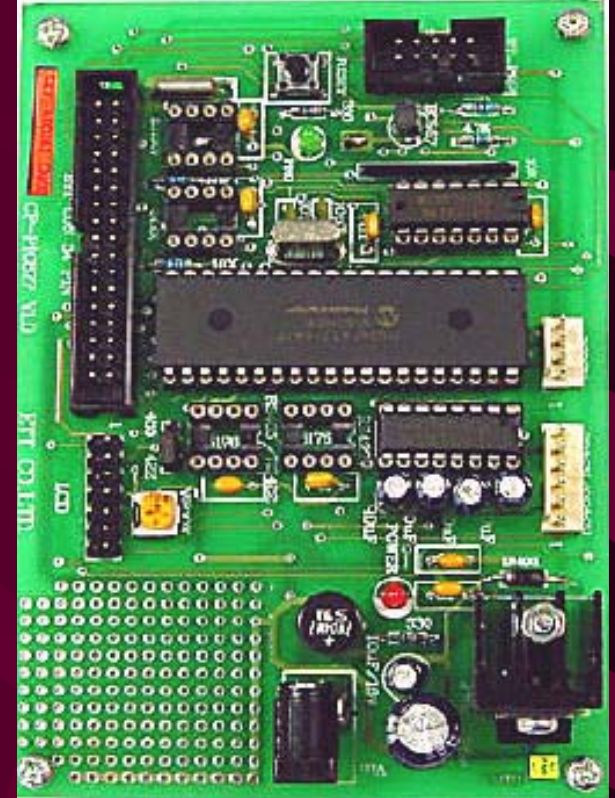


# การใช้งาน CP-PIC877 V1.0



บริษัท อีทีที จำกัด



CP-PIC877 V1.0



## คุณสมบัติทั่วไปของ CPU PIC 16F877



- 35 Instruction คำสั่ง
- ปฏิบัติคำสั่งทั่วไปใน Cycle เดียว และ 2 Cycle ในคำสั่งการกระโดด
- ทำงานที่ความถี่สูงสุด 20 MHz (16F877-20/P)
- หน่วยความจำโปรแกรม 8 K(14 Bit Words)
- หน่วยความจำข้อมูล (RAM) 368 Byte
- EEPROM 256 Byte
- สามารถตอบสนองอินเทอร์รัพท์ 14 แหล่ง
- STACK 8 ระดับ
- POR, BOR, PWRT , Oscillator Start-Up Timer และ Watchdog Timer
- Code Protection

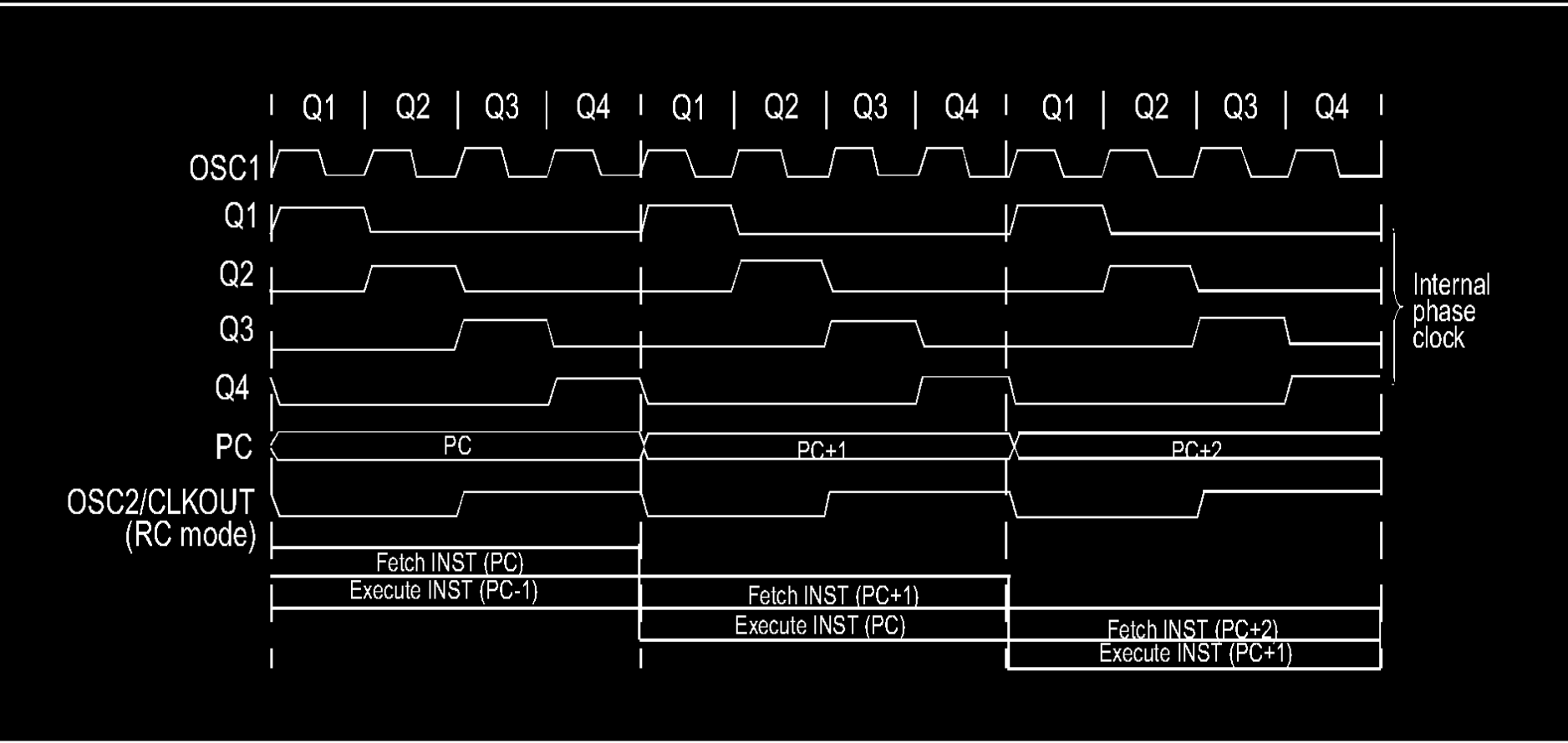




- Sleep Mode
- สามารถเลือกโหมดของสัญญาณพิก้าได้
- In-Circuit Serial Programming (ICSP)
- สามารถโปรแกรมได้ ด้วยแรงดัน +5V
- ทำงานได้ที่ไฟเลี้ยง 2.0 V- 5.5 V
- กระแสทั้งซิงก์ และ ซอร์สของพอร์ต คือ 25 mA
- Timer/Counter 3 ตัว Timer0,Timer1 และ Timer2
- โมดูล Capture/Compare/PWM จำนวน 2 ชุด
- USART
- Analog to Digital Converter 10Bit 8 Channel
- พอร์ต I/O จำนวน 5 พอร์ต A,B,C,D และ E รวมทั้งสิ้น 33 Bit



FIGURE 3-2: CLOCK/INSTRUCTION CYCLE

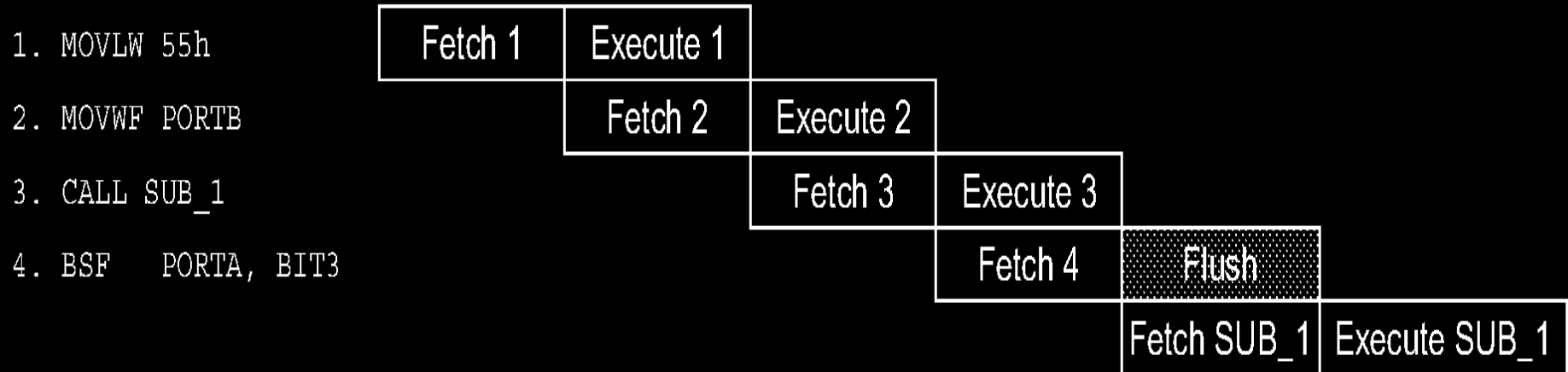


$$4\text{Mhz} / 4 = 1\text{Mhz}$$

$$1/1\text{Mhz} = 1\mu\text{S}$$



## EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



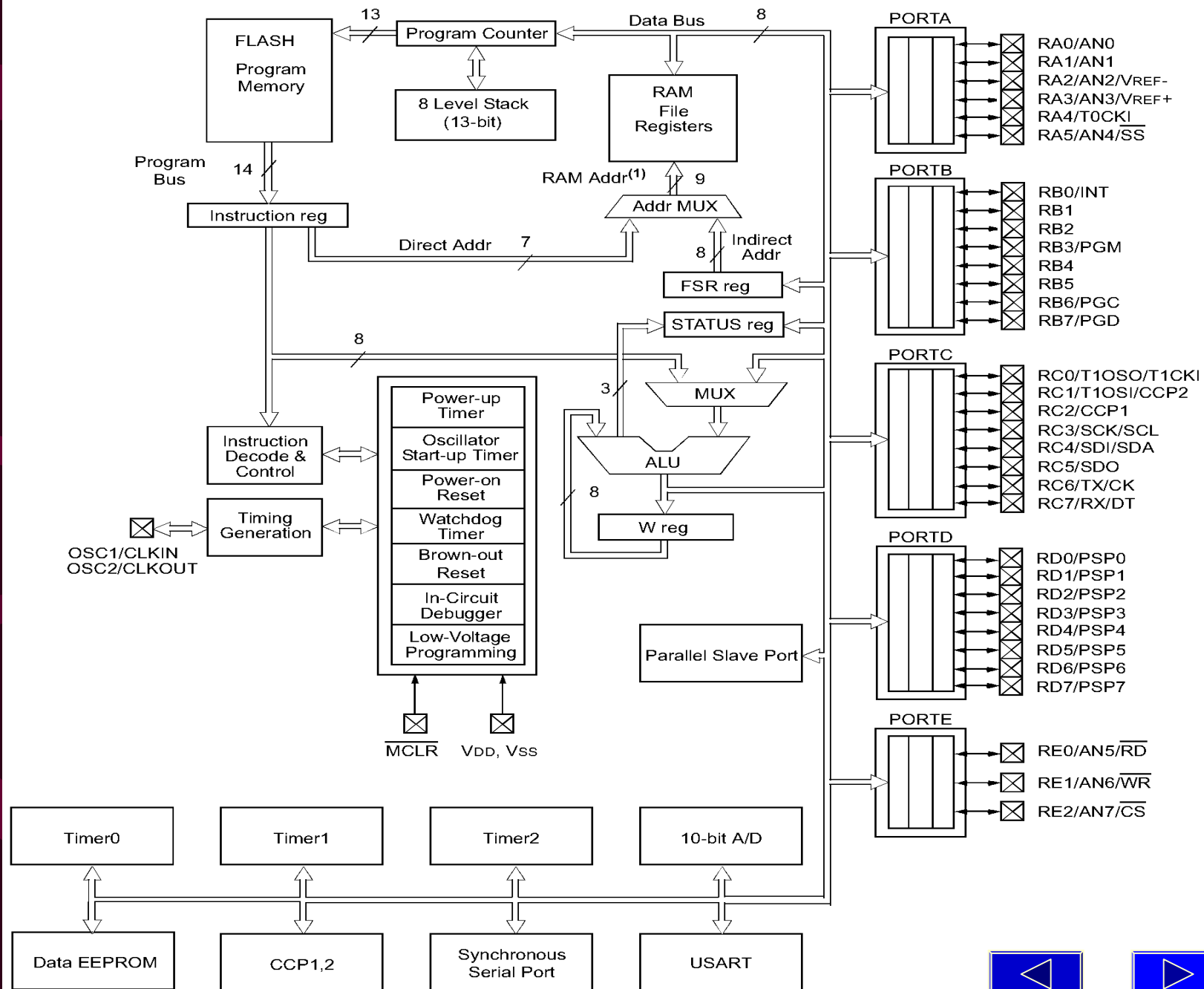
All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is “flushed” from the pipeline while the new instruction is being fetched and then executed.



|                                          |                                      |
|------------------------------------------|--------------------------------------|
| <input type="checkbox"/> MCLR/VPP        | <input type="checkbox"/> RB7/PGD     |
| <input type="checkbox"/> RA0/AN0         | <input type="checkbox"/> RB6/PGC     |
| <input type="checkbox"/> RA1/AN1         | <input type="checkbox"/> RB5         |
| <input type="checkbox"/> RA2/AN2/VREF-   | <input type="checkbox"/> RB4         |
| <input type="checkbox"/> RA3/AN3/VREF+   | <input type="checkbox"/> RB3/PGM     |
| <input type="checkbox"/> RA4/T0CKI       | <input type="checkbox"/> RB2         |
| <input type="checkbox"/> RA5/SS/AN4      | <input type="checkbox"/> RB1         |
| <input type="checkbox"/> RE0/RD/AN5      | <input type="checkbox"/> RB0/INT     |
| <input type="checkbox"/> RE1/WR/AN6      | <input type="checkbox"/> VDD         |
| <input type="checkbox"/> RE2/CS/AN7      | <input type="checkbox"/> VSS         |
| <input type="checkbox"/> VDD             | <input type="checkbox"/> RD7/PSP7    |
| <input type="checkbox"/> VSS             | <input type="checkbox"/> RD6/PSP6    |
| <input type="checkbox"/> OSC1/CLKIN      | <input type="checkbox"/> RD5/PSP5    |
| <input type="checkbox"/> OSC2/CLKOUT     | <input type="checkbox"/> RD4/PSP4    |
| <input type="checkbox"/> RC0/T1OSO/T1CKI | <input type="checkbox"/> RC7/RX/DT   |
| <input type="checkbox"/> RC1/T1OSI/CCP2  | <input type="checkbox"/> RC6/TX/CK   |
| <input type="checkbox"/> RC2/CCP1        | <input type="checkbox"/> RC5/SDO     |
| <input type="checkbox"/> RC3/SCK/SCL     | <input type="checkbox"/> RC4/SDI/SDA |
| <input type="checkbox"/> RD0/PSP0        | <input type="checkbox"/> RD3/PSP3    |
| <input type="checkbox"/> RD1/PSP1        | <input type="checkbox"/> RD2/PSP2    |

**PIC16F877**





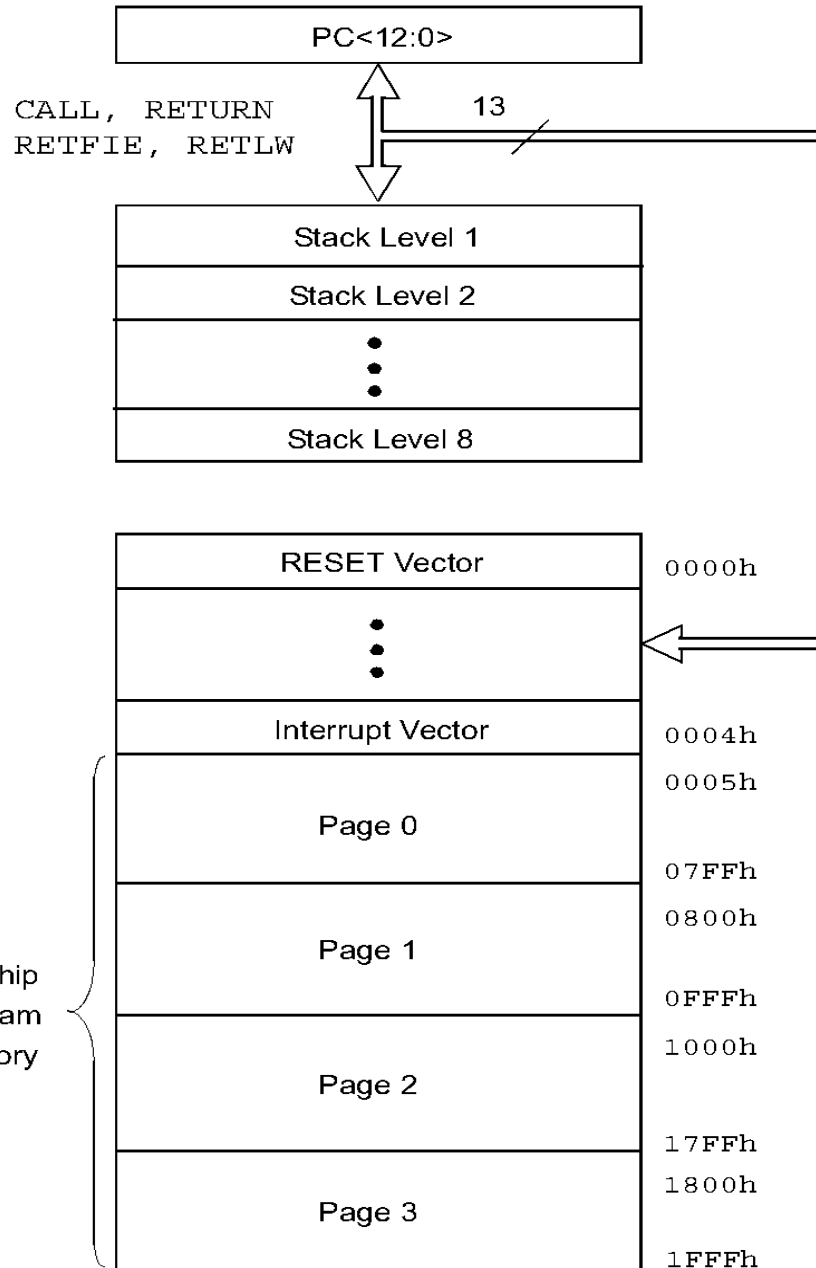


## การจัดสรรพื้นที่หน่วยความจำ และ รีจิสเตอร์ต่างๆ

1. หน่วยความจำโปรแกรม 8 Kwords
2. หน่วยความจำข้อมูล RAM 368 Byte
3. หน่วยความจำข้อมูล EEPROM 256 Byte



# หน่วยความจำโปรแกรม



# หน่วยความจำข้อมูล

| File Address                      | File Address                      | File Address                      | File Address                      |
|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| Indirect addr. <sup>(*)</sup>     | Indirect addr. <sup>(*)</sup>     | Indirect addr. <sup>(*)</sup>     | Indirect addr. <sup>(*)</sup>     |
| TMR0                              | OPTION_REG                        | TMR0                              | OPTION_REG                        |
| PCL                               | PCL                               | PCL                               | PCL                               |
| STATUS                            | STATUS                            | STATUS                            | STATUS                            |
| FSR                               | FSR                               | FSR                               | FSR                               |
| PORTA                             | TRISA                             |                                   |                                   |
| PORTB                             | TRISB                             | PORTB                             | TRISB                             |
| PORTC                             | TRISC                             |                                   |                                   |
| PORTD <sup>(1)</sup>              | TRISD <sup>(1)</sup>              |                                   |                                   |
| PORTE <sup>(1)</sup>              | TRISE <sup>(1)</sup>              |                                   |                                   |
| PCLATH                            | PCLATH                            | PCLATH                            | PCLATH                            |
| INTCON                            | INTCON                            | INTCON                            | INTCON                            |
| PIR1                              | PIE1                              | EEDATA                            | EECON1                            |
| PIR2                              | PIE2                              | EEADR                             | EECON2                            |
| TMR1L                             | PCON                              | EEDATH                            | Reserved <sup>(2)</sup>           |
| TMR1H                             |                                   | EEADRH                            | Reserved <sup>(2)</sup>           |
| T1CON                             |                                   |                                   |                                   |
| TMR2                              | SSPCON2                           |                                   |                                   |
| T2CON                             | PR2                               |                                   |                                   |
| SSPBUF                            | SSPADDD                           |                                   |                                   |
| SSPCON                            | SSPSTAT                           |                                   |                                   |
| CCPR1L                            |                                   |                                   |                                   |
| CCPR1H                            |                                   |                                   |                                   |
| CCP1CON                           |                                   |                                   |                                   |
| RCSTA                             | TXSTA                             | General Purpose Register 16 Bytes | General Purpose Register 16 Bytes |
| TXREG                             | SPBRG                             |                                   |                                   |
| RCREG                             |                                   |                                   |                                   |
| CCPR2L                            |                                   |                                   |                                   |
| CCPR2H                            |                                   |                                   |                                   |
| CCP2CON                           |                                   |                                   |                                   |
| ADRESH                            | ADRESL                            |                                   |                                   |
| ADCON0                            | ADCON1                            |                                   |                                   |
|                                   |                                   |                                   |                                   |
| General Purpose Register 96 Bytes | General Purpose Register 80 Bytes | General Purpose Register 80 Bytes | General Purpose Register 80 Bytes |
|                                   | accesses 70h-7Fh                  | accesses 70h-7Fh                  | accesses 70h - 7Fh                |
| Bank 0                            | Bank 1                            | Bank 2                            | Bank 3                            |



# STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

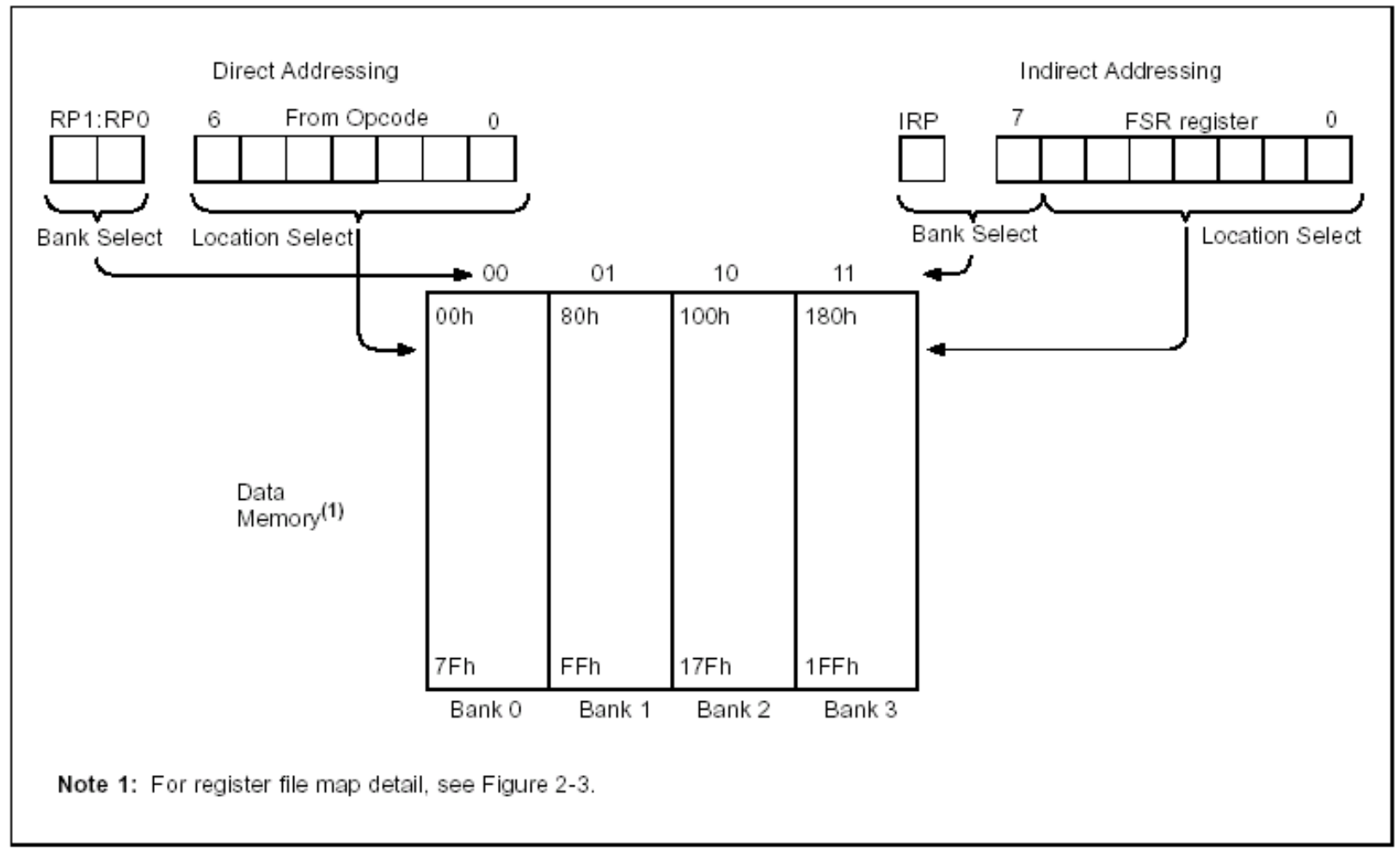
|       |       |       |                 |                 |       |       |       |
|-------|-------|-------|-----------------|-----------------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R-1             | R-1             | R/W-x | R/W-x | R/W-x |
| IRP   | RP1   | RP0   | $\overline{TO}$ | $\overline{PD}$ | Z     | DC    | C     |
| bit 7 |       |       | bit 0           |                 |       |       |       |

| RP1 | RP0 | Bank Select          |
|-----|-----|----------------------|
| 0   | 0   | Bank 0 : 00h - 7Fh   |
| 0   | 1   | Bank 1 : 80h - FFh   |
| 1   | 0   | Bank 2 : 100h - 17Fh |
| 1   | 1   | Bank 3 : 180h – 1FFh |



# DIRECT/INDIRECT ADDRESSING

FIGURE 2-6: DIRECT/INDIRECT ADDRESSING



|          |       |       |                      |
|----------|-------|-------|----------------------|
|          | MOVLW | 0X20  | ; Initialize pointer |
|          | MOVWF | FSR   | ; to RAM             |
| NEXT     | CLRF  | INDF  | ; clear INDF         |
|          | INCF  | FSR,F | ; inc pointer        |
|          | BTFSS | FSR,4 | ; all done?          |
|          | GOTO  | NEXT  | ; no clear next      |
| CONTINUE |       |       |                      |
|          | :     |       | ; Yes continue       |





### 3. หน่วยความจำข้อมูล EEPROM

มี จำนวน 256 ไบต์ สามารถอ่านและเขียนได้ โดยผ่าน  
รีจิสเตอร์ฟังก์ชันพิเศษ 4 ตัวคือ

**EECON1** : ควบคุมการเข้าถึงหน่วยความจำ

**EECON2** : จัดลำดับการเขียนข้อมูล

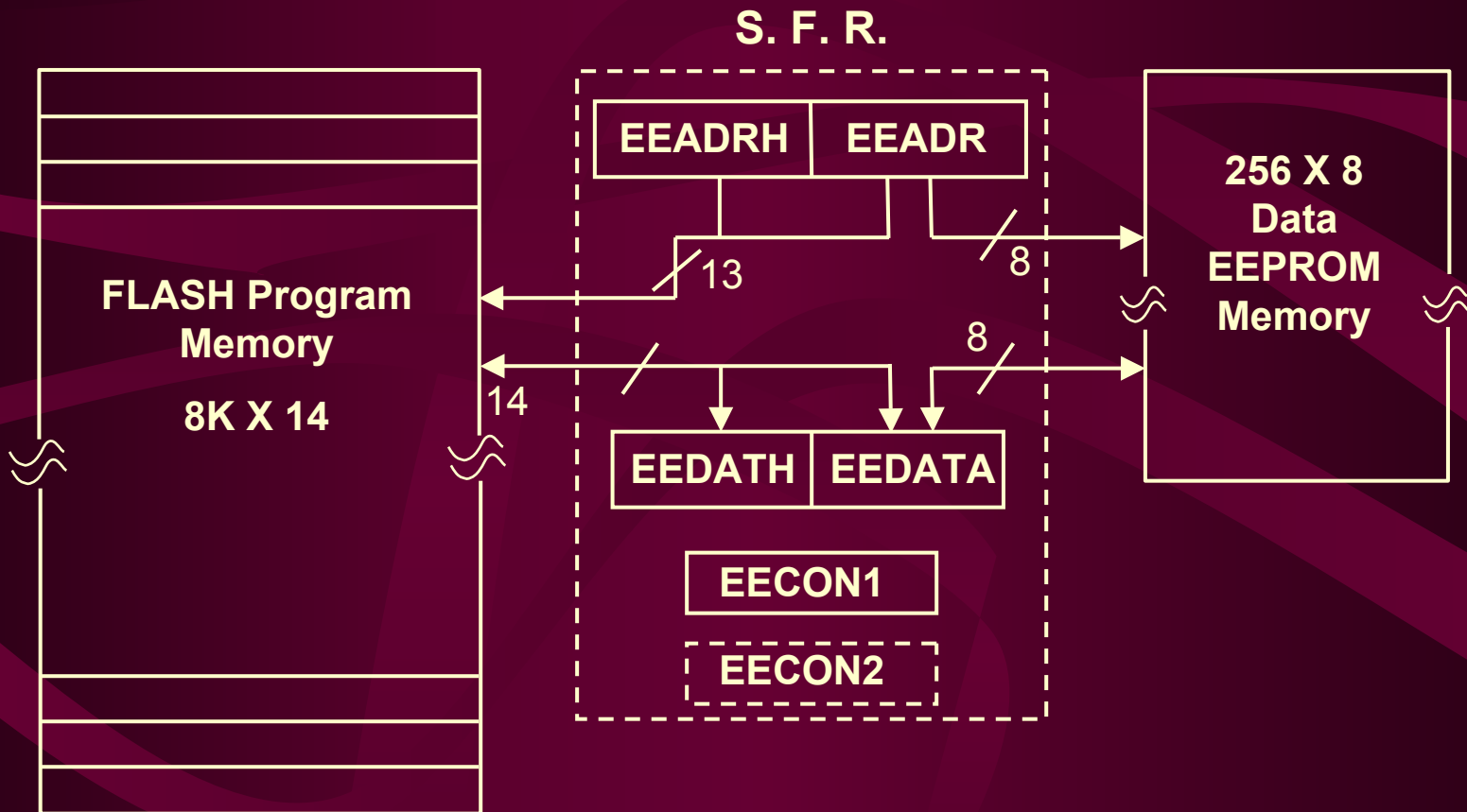
**EEDATA** : เป็นบัฟเฟอร์ใช้เก็บข้อมูล 8 บิต สำหรับการอ่านและเขียน

**EEADR** : รีจิสเตอร์สำหรับเก็บแอดเดรส 00h – FFh (256 Byte)





# FLASH Program and Data EEPROM Memory



# FLASH Program & Data EEPROM: EECON1 Register

|       |   |   |   |       |      |    |      |
|-------|---|---|---|-------|------|----|------|
| EEPGD | - | - | - | WRERR | WREN | WR | RD   |
| bit7  |   |   |   |       |      |    | bit0 |

**EEPGD: Program / Data EEPROM Select Bit**

1 = Accesses Program Memory

0 = Accesses Data Memory

**WRERR: EEPROM Error Flag Bit**

1 = A write operation is prematurely terminated

0 = The write operation completed

**WREN: EEPROM Write Enable Bit**

1 = Allows write cycles

0 = Inhibits write to the EEPROM

**WR: Write Control Bit**

1 = Initiates a write cycle (cleared by hardware only)

0 = Write cycle to the EEPROM is complete

**RD: Read Control Bit**

1 = Initiates a read cycle (cleared by hardware only)

0 = Read cycle from the EEPROM is complete



# รีจิสเตอร์ STATUS

|       |       |       |                 |                 |       |       |       |
|-------|-------|-------|-----------------|-----------------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R-1             | R-1             | R/W-x | R/W-x | R/W-x |
| IRP   | RP1   | RP0   | $\overline{TO}$ | $\overline{PD}$ | Z     | DC    | C     |
| bit 7 |       |       |                 |                 |       |       |       |
|       |       |       |                 |                 |       |       |       |
|       |       |       |                 |                 |       |       | bit 0 |

|         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 7   | <b>IRP:</b> Register Bank Select bit (used for indirect addressing)<br>1 = Bank 2, 3 (100h - 1FFh)<br>0 = Bank 0, 1 (00h - FFh)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| bit 6-5 | <b>RP1:RP0:</b> Register Bank Select bits (used for direct addressing)<br>11 = Bank 3 (180h - 1FFh)<br>10 = Bank 2 (100h - 17Fh)<br>01 = Bank 1 (80h - FFh)<br>00 = Bank 0 (00h - 7Fh)<br>Each bank is 128 bytes                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| bit 4   | <b><math>\overline{TO}</math>:</b> Time-out bit<br>1 = After power-up, CLRWDI instruction, or SLEEP instruction<br>0 = A WDT time-out occurred                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| bit 3   | <b><math>\overline{PD}</math>:</b> Power-down bit<br>1 = After power-up or by the CLRWDI instruction<br>0 = By execution of the SLEEP instruction                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| bit 2   | <b>Z:</b> Zero bit<br>1 = The result of an arithmetic or logic operation is zero<br>0 = The result of an arithmetic or logic operation is not zero                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| bit 1   | <b>DC:</b> Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)<br>(for borrow, the polarity is reversed)<br>1 = A carry-out from the 4th low order bit of the result occurred<br>0 = No carry-out from the 4th low order bit of the result                                                                                                                                                                                                                                                                                                                                                                                                |
| bit 0   | <b>C:</b> Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)<br>1 = A carry-out from the Most Significant bit of the result occurred<br>0 = No carry-out from the Most Significant bit of the result occurred<br><br><b>Note:</b> For borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instruction  is loaded with either the high, or low order bit of the source register.  |

# รีจิสเตอร์ OPTION



|       |        |       |       |       |       |       |       |
|-------|--------|-------|-------|-------|-------|-------|-------|
| R/W-1 | R/W-1  | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| RBPU  | INTEDG | T0CS  | T0SE  | PSA   | PS2   | PS1   | PS0   |
| bit 7 |        |       |       | bit 0 |       |       |       |

- bit 7 **RBPU**: PORTB Pull-up Enable bit  
 1 = PORTB pull-ups are disabled  
 0 = PORTB pull-ups are enabled by individual port latch values
- bit 6 **INTEDG**: Interrupt Edge Select bit  
 1 = Interrupt on rising edge of RB0/INT pin  
 0 = Interrupt on falling edge of RB0/INT pin
- bit 5 **T0CS**: TMR0 Clock Source Select bit  
 1 = Transition on RA4/T0CKI pin  
 0 = Internal instruction cycle clock (CLKOUT)
- bit 4 **T0SE**: TMR0 Source Edge Select bit  
 1 = Increment on high-to-low transition on RA4/T0CKI pin  
 0 = Increment on low-to-high transition on RA4/T0CKI pin
- bit 3 **PSA**: Prescaler Assignment bit  
 1 = Prescaler is assigned to the WDT  
 0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS2:PS0**: Prescaler Rate Select bits

| Bit Value | TMR0 Rate | WDT Rate |
|-----------|-----------|----------|
| 000       | 1 : 2     | 1 : 1    |
| 001       | 1 : 4     | 1 : 2    |
| 010       | 1 : 8     | 1 : 4    |
| 011       | 1 : 16    | 1 : 8    |
| 100       | 1 : 32    | 1 : 16   |
| 101       | 1 : 64    | 1 : 32   |
| 110       | 1 : 128   | 1 : 64   |
| 111       | 1 : 256   | 1 : 128  |



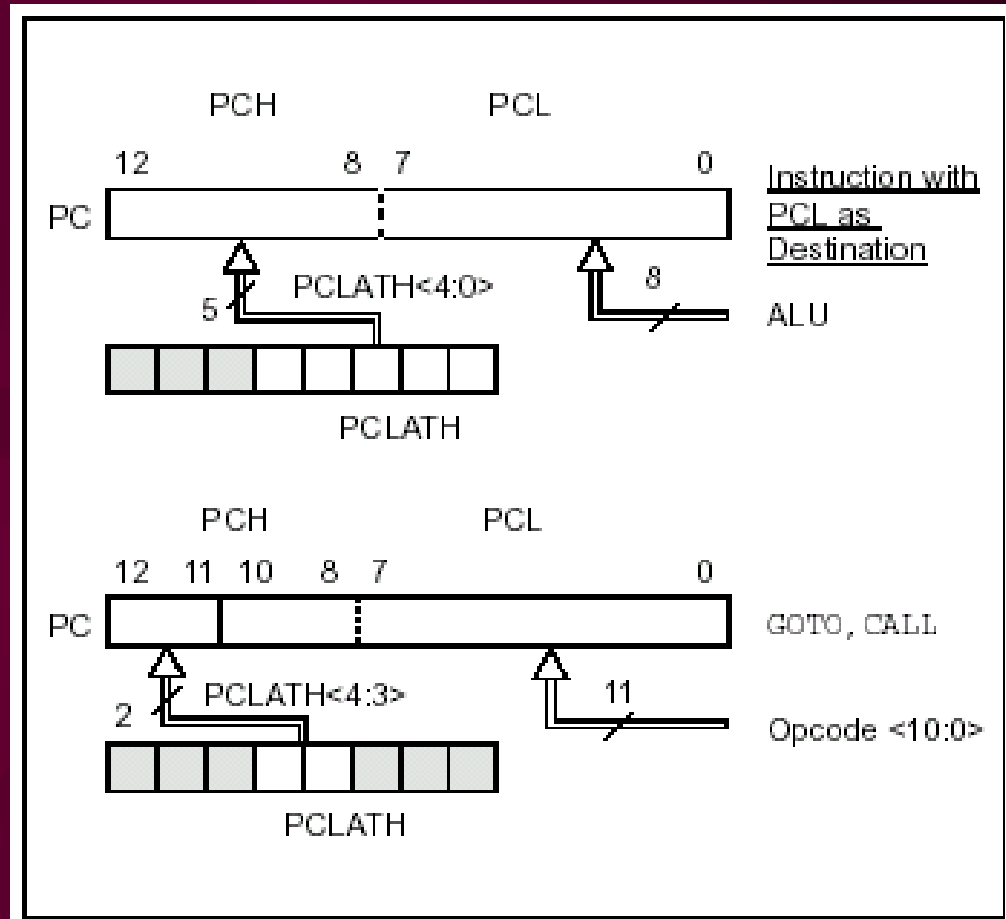
## รีจิสเตอร์ W (Working Register)

## รีจิสเตอร์ PC (Program Counter)



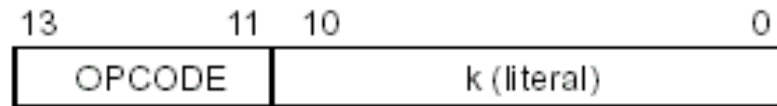
$$2^{13} = 8192 \text{ (8KByte)}$$

$$2^{11} = 2048 \text{ (2KByte)}$$





CALL and GOTO instructions only



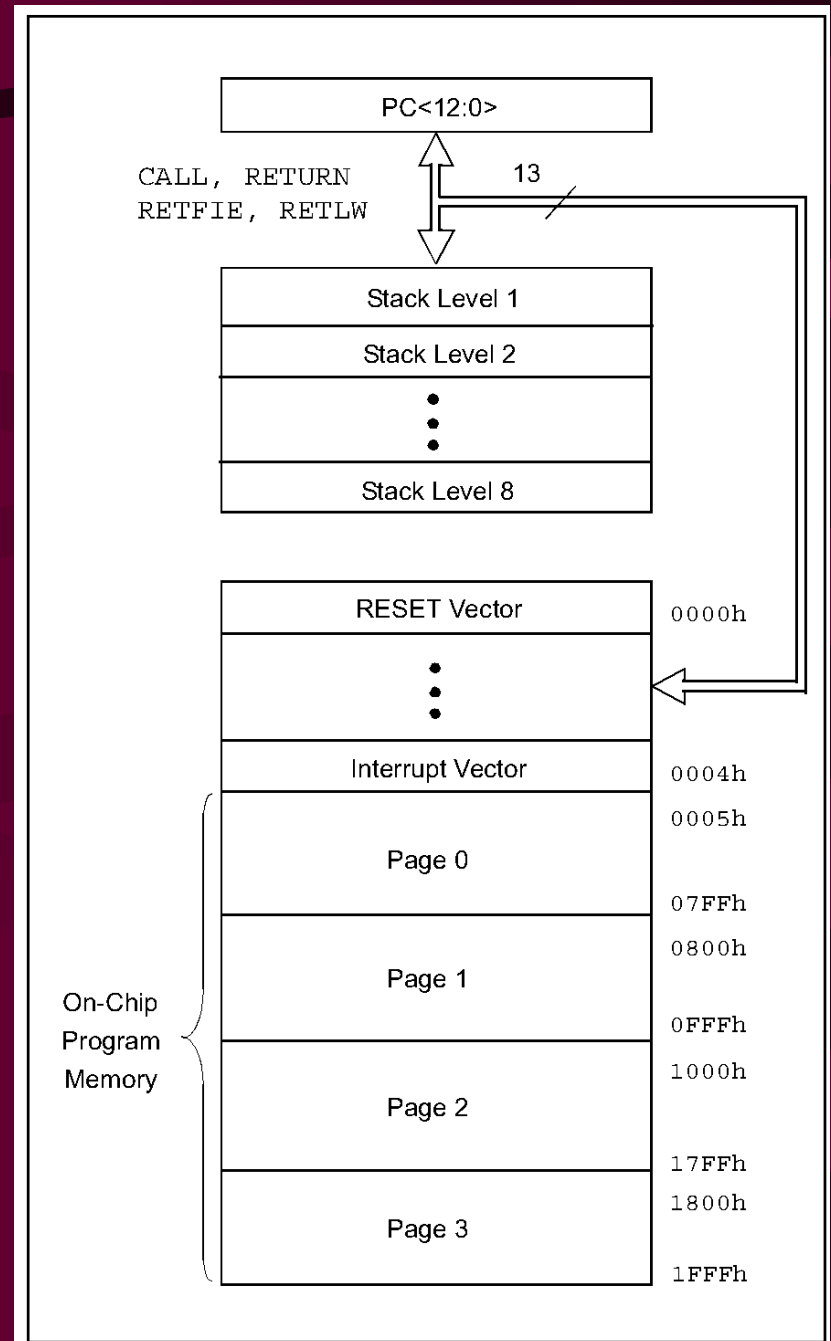
k = 11-bit immediate value

```
ORG 0x500
BCF PCLATH,4
BSF PCLATH,3 ;Select page 1
                ; (800h-FFFh)
CALL SUB1_P1   ;Call subroutine in
:              ;page 1 (800h-FFFh)
:
ORG 0x900      ;page 1 (800h-FFFh)
SUB1_P1
:              ;called subroutine
                ;page 1 (800h-FFFh)
:
RETURN         ;return to
                ;Call subroutine
                ;in page 0
                ; (000h-7FFh)
```

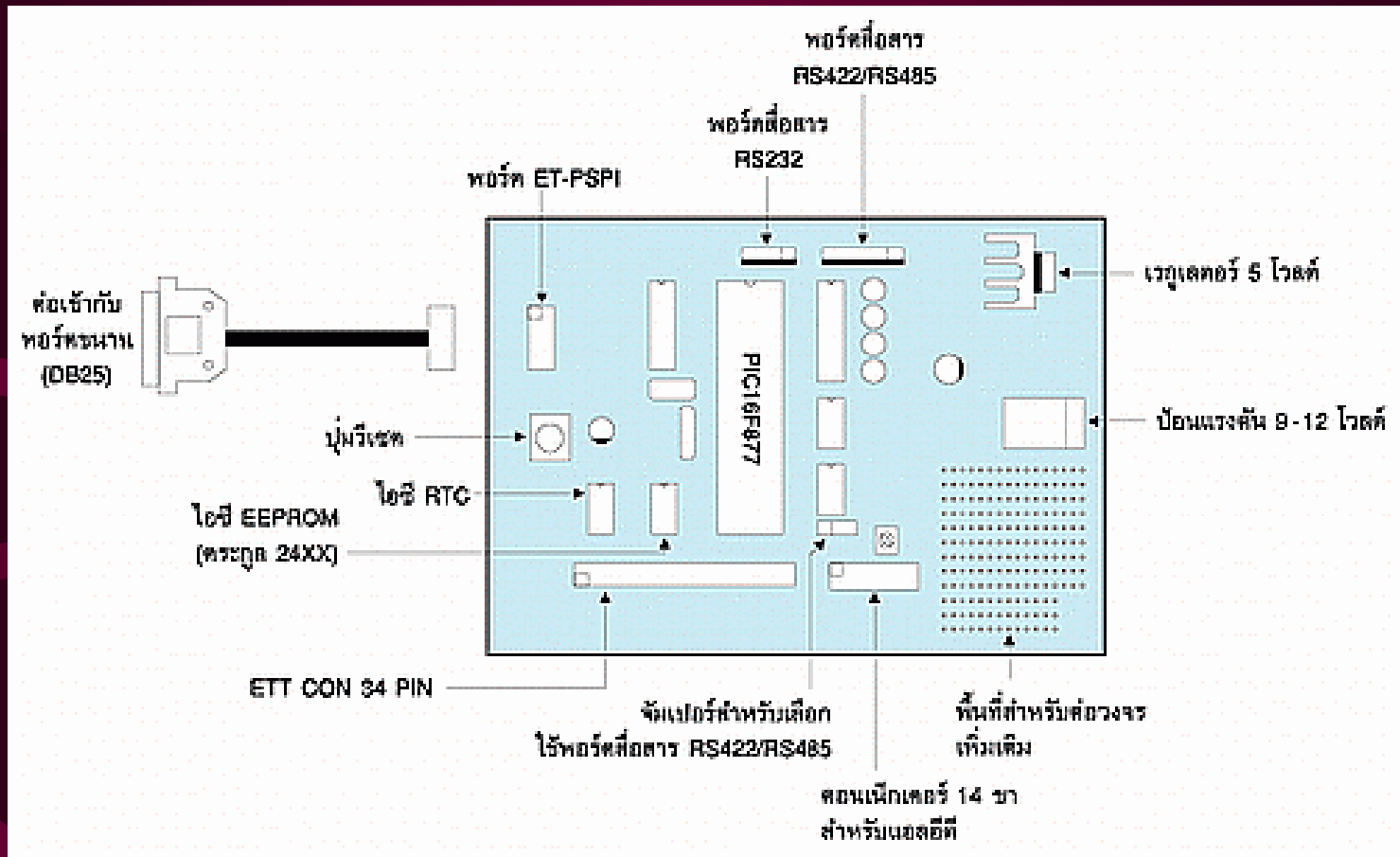


# Program Memory

| PCLATH<4> | PCLATH<3> | Page   |
|-----------|-----------|--------|
| 0         | 0         | Page 0 |
| 0         | 1         | Page 1 |
| 1         | 0         | Page 2 |
| 1         | 1         | Page 3 |

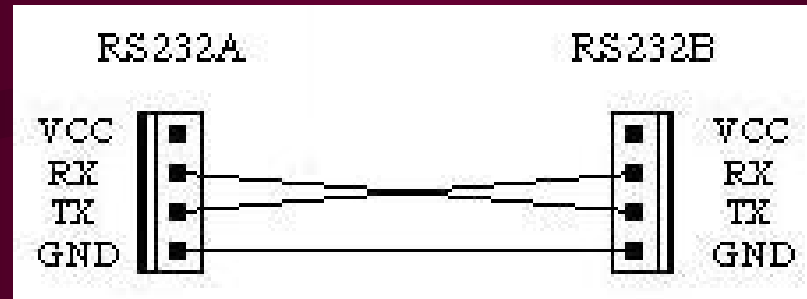


## ส่วนประกอบและข้อจำกัดต่างๆ ของบอร์ด CP-PIC877 V1.0

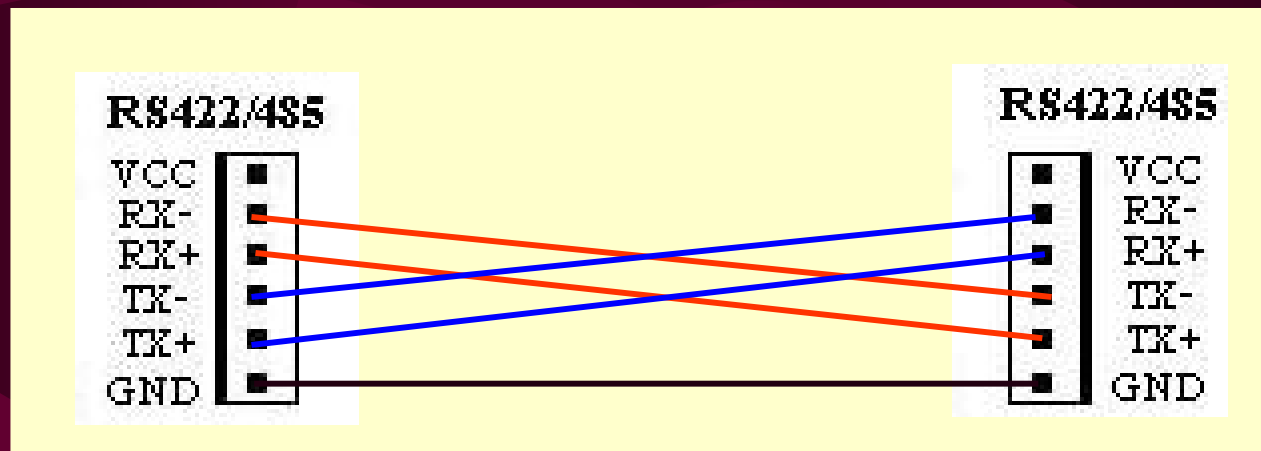




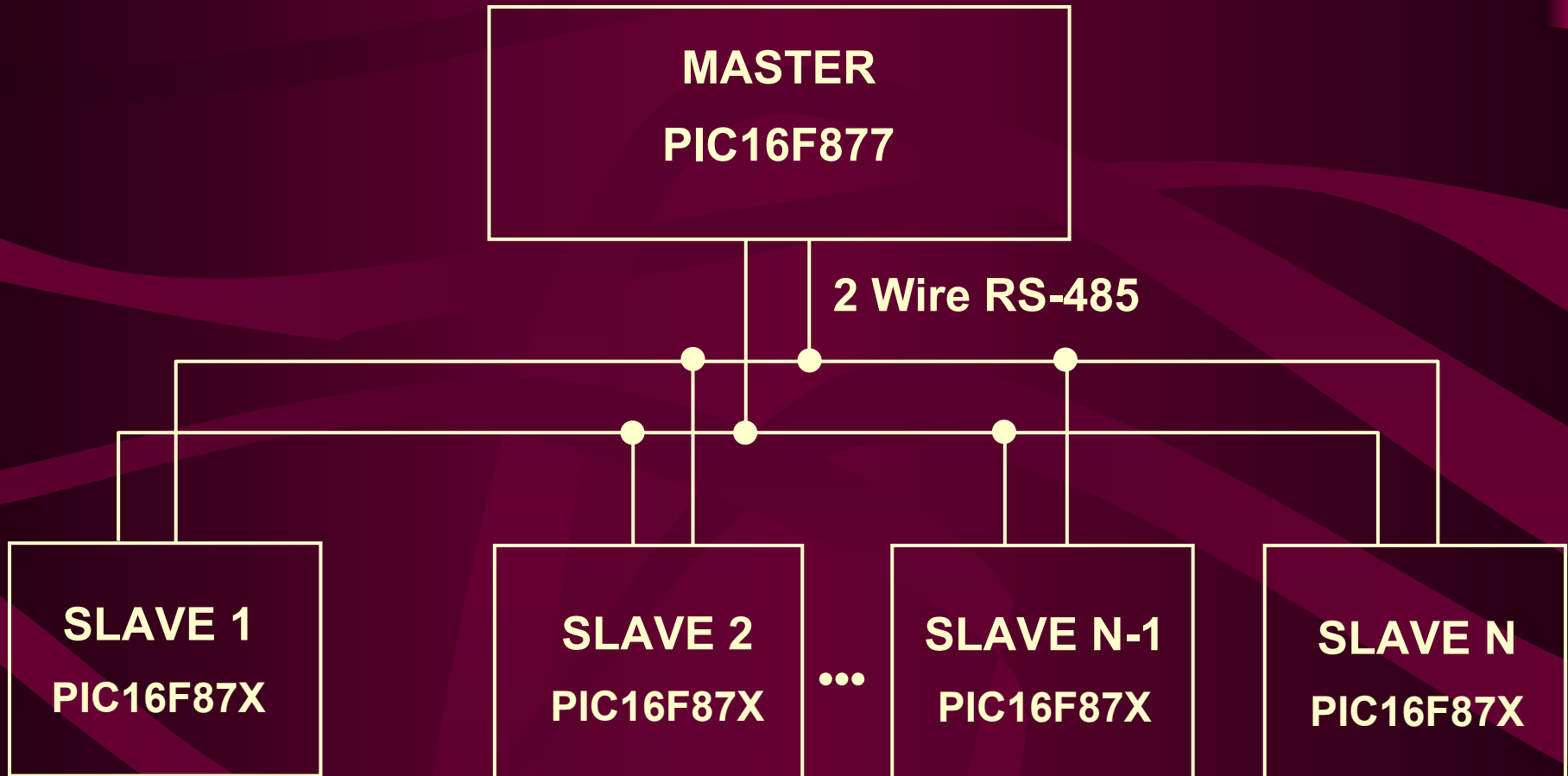
## RS-232

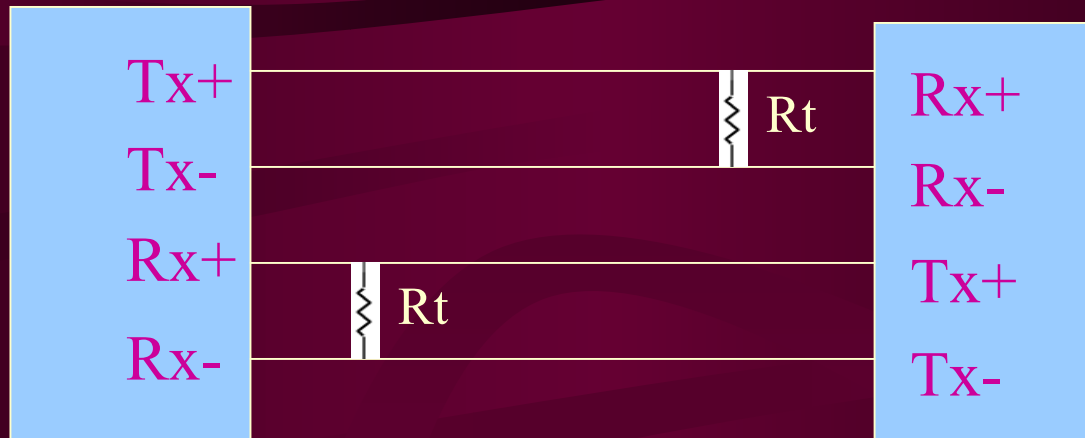


## RS-422/RS-485

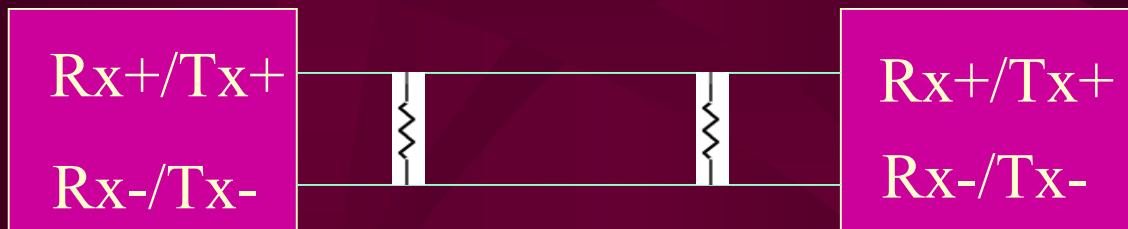


# Addressable USART: Multi-Drop Serial Interface





การต่อ RS-422 แบบ Full Duplex



การต่อ RS-485 แบบ Half Duplex



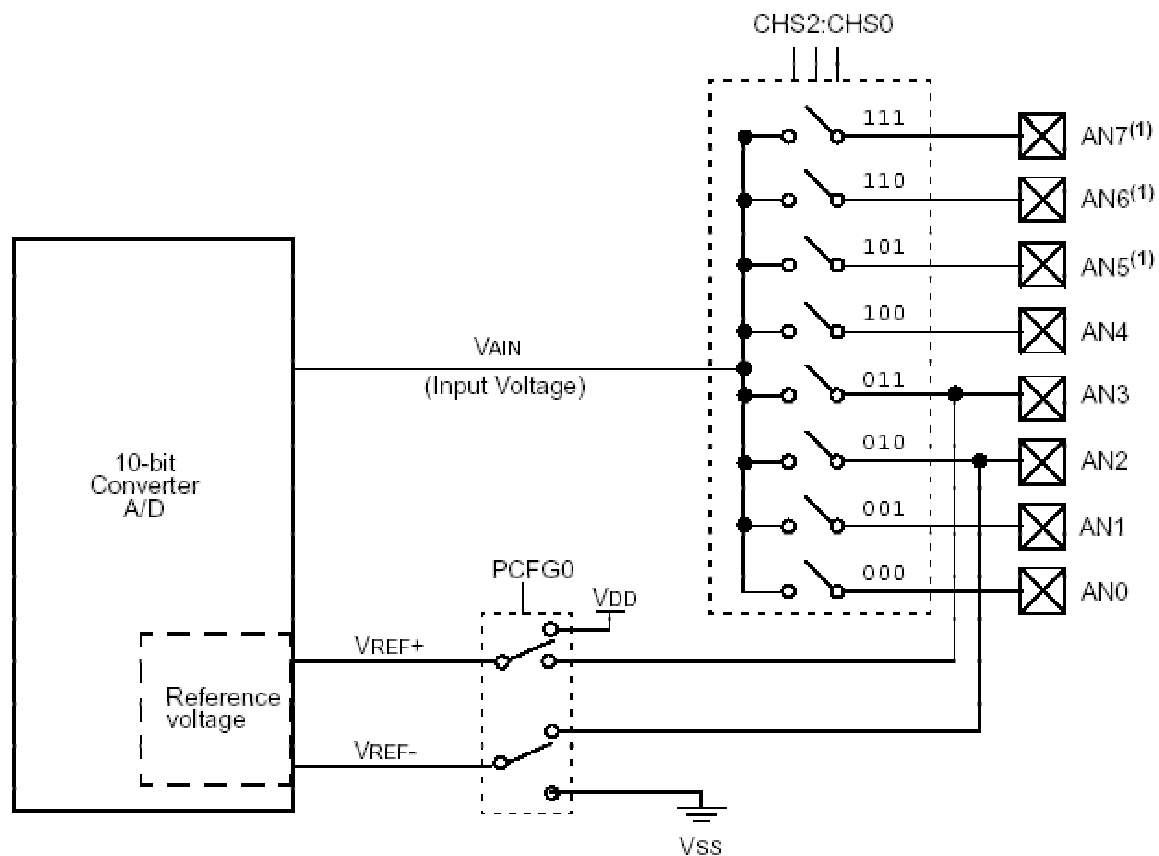
# 10-Bit A/D Module: Features



PIC16F87X devices have a 10-bit A/D ( $\pm 1$  LSB)

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register0 (ADCON0)
- A/D Control Register1 (ADCON1)



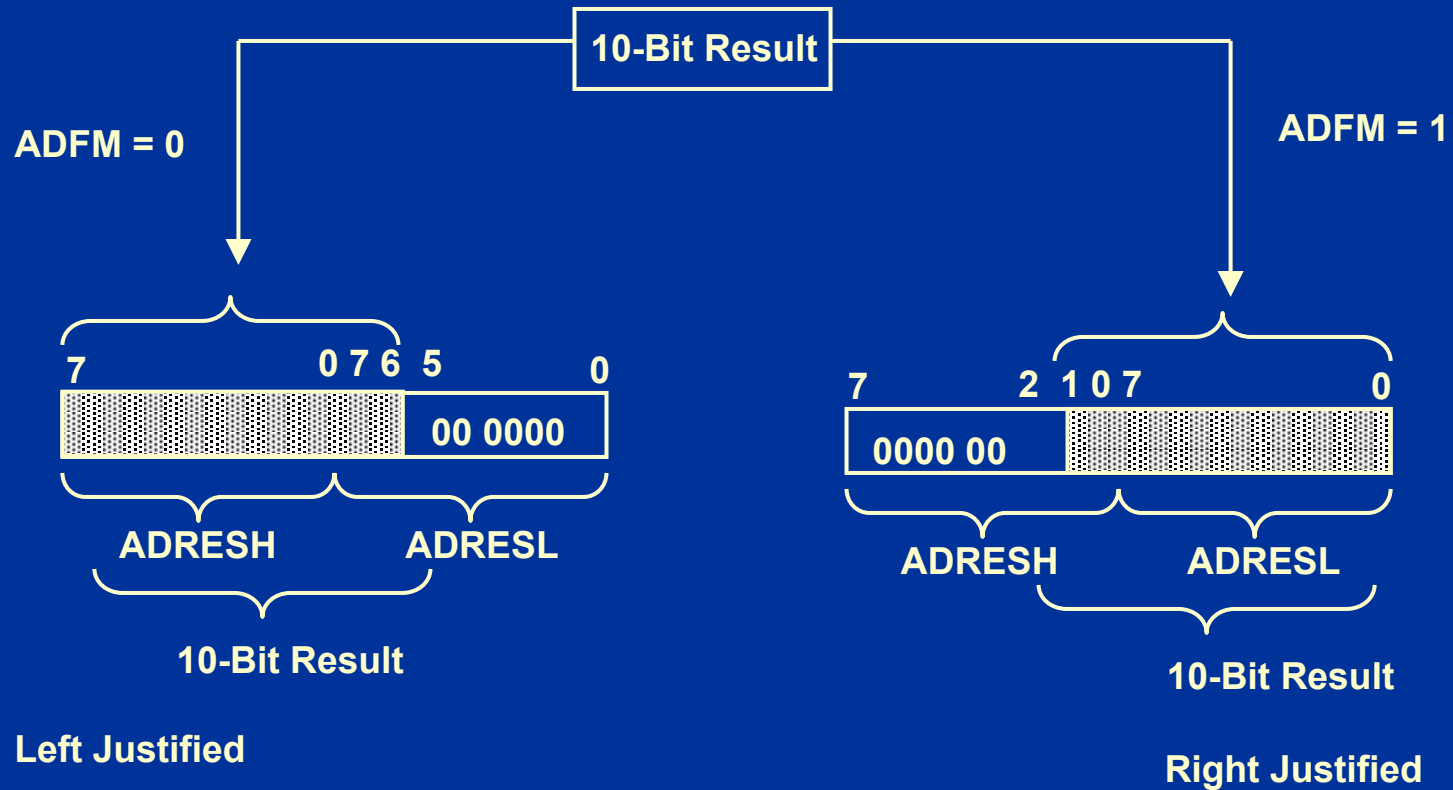


- Note** 1: Channels AN5 through AN7 are not available on PIC18F2X8 devices.
- 2: All I/O pins have diode protection to VDD and VSS.

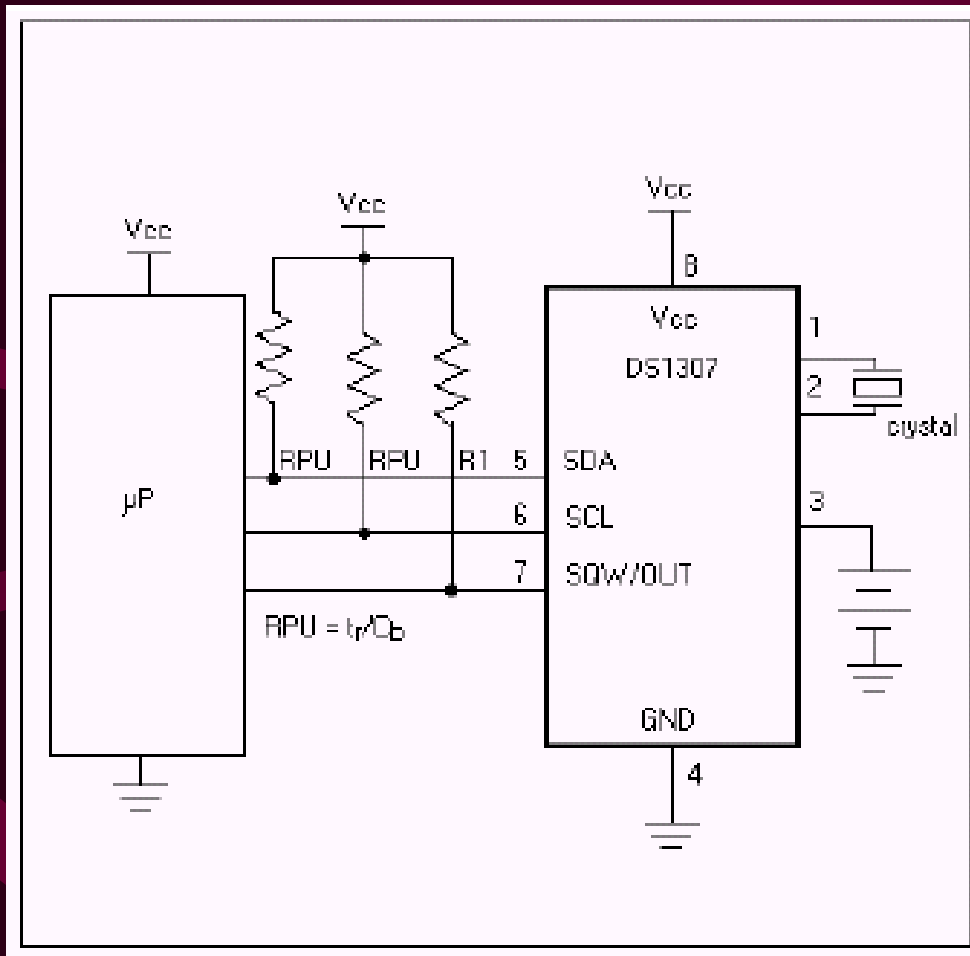


# 10-Bit A/D Module:

## Left/Right Justification of A/D Result



# RTC (Real Time Clock) #DS1307



00H

SECONDS

MINUTES

HOURS

DAY

DATE

MONTH

YEAR

CONTROL

07H

08H

RAM

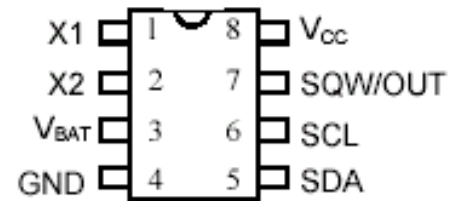
56 x 8

3FH

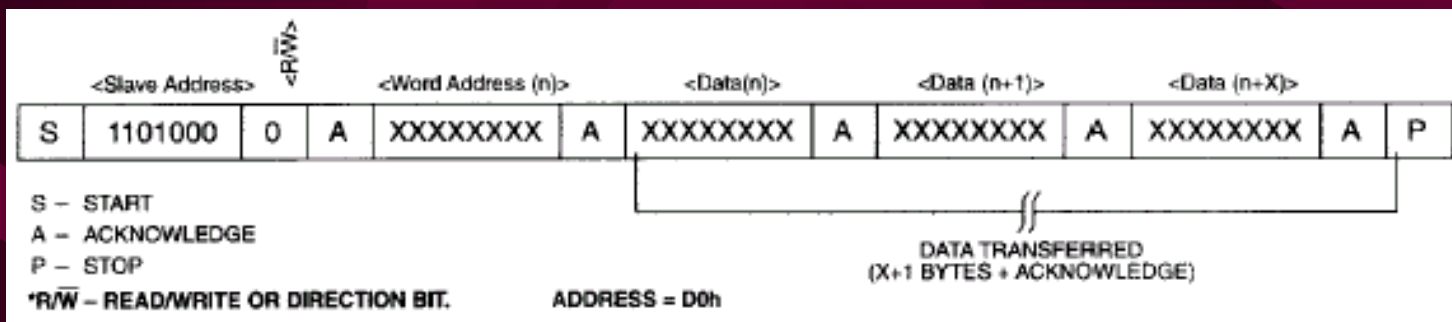
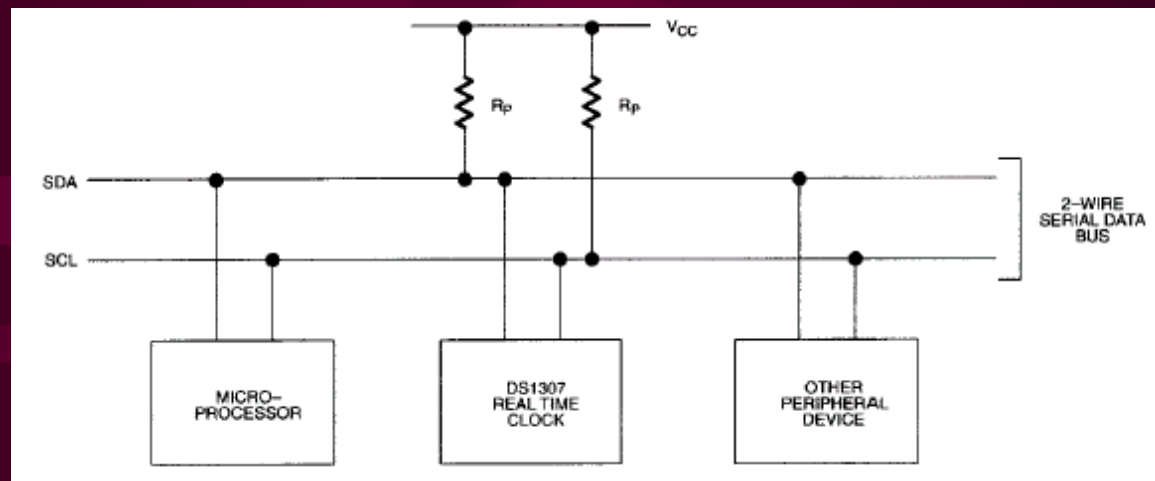




# PIN ASSIGNMENT



DS1307 8-Pin DIP (300-mil)



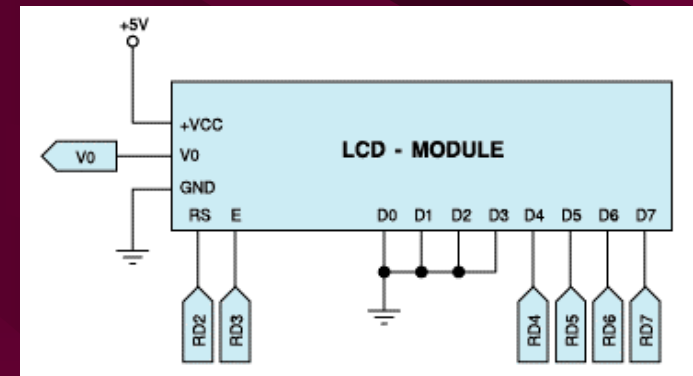
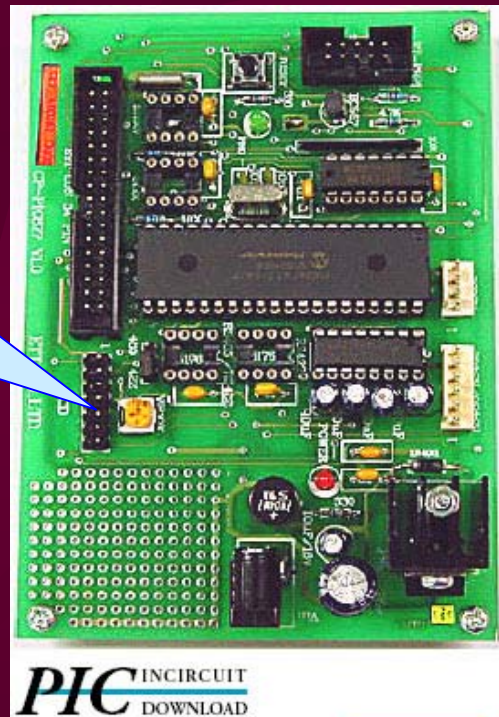
# EEPROM 24XX



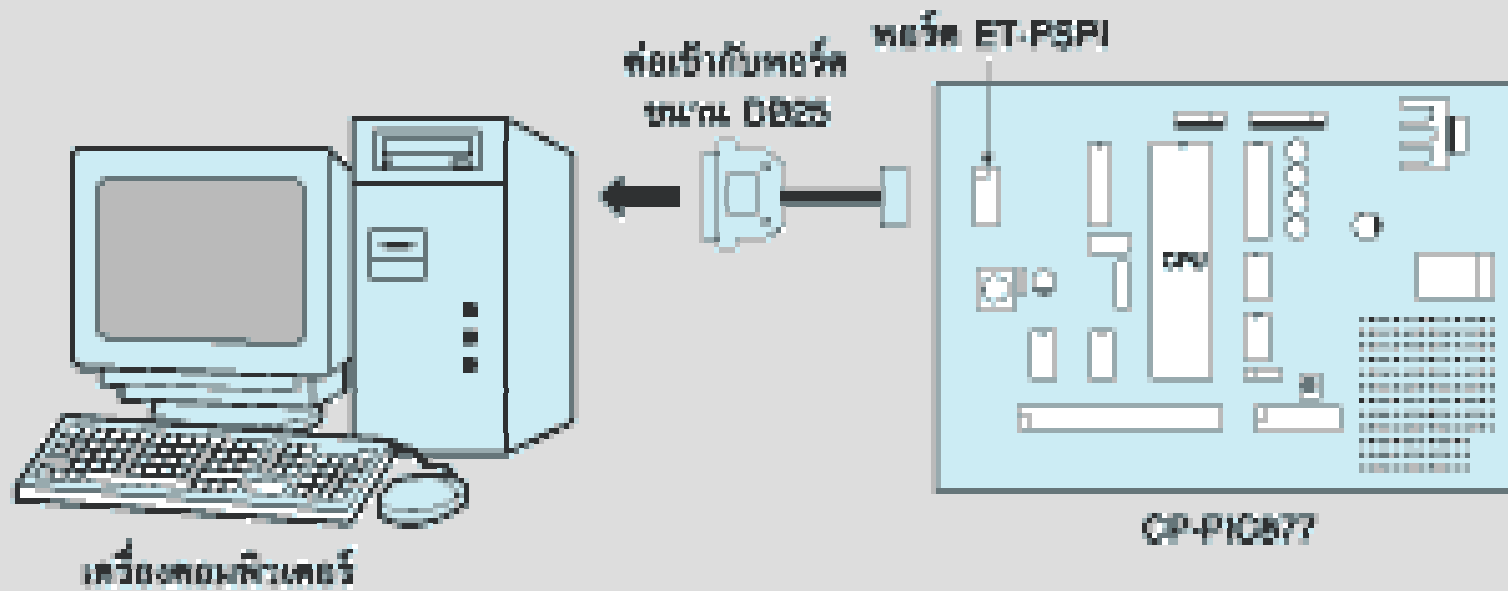
การต่อจะต่อผ่านระบบบัสของ I2CBUS เหมือนกับ RTC แต่  
การรับส่งข้อมูลจะไม่เกิดปัญหา เนื่องจาก อุปกรณ์ทั้งสองจะมี  
แอดเดรสต่างกัน

## LCD 14 PIN

|         |     |         |
|---------|-----|---------|
| 2. +Vcc | ● ● | 1. GND  |
| 4. RS   | ● ● | 3. Vo   |
| 5. GND  | ● ● | 6. R/W  |
| 7. GND  | ● ● | 8. GND  |
| 9. GND  | ● ● | 10. GND |
| 11. D4  | ● ● | 12. D5  |
| 13. D6  | ● ● | 14. D7  |



# การดาวน์โหลดโปรแกรม



## DESTINATION PROFILE

- ▲ INTRODUCTORY SEMINARS
- ▲ ADVANCED SEMINARS
- ▲ INTRODUCTORY WORKSHOP
- ▲ FLASH/ANALOG WORKSHOP
- ▲ PIC/FLUXY WORKSHOP
- ▲ PIC/SOCKET WORKSHOP

ROM OTP FLASH  
AVAILABLE AVAILABLE AVAILABLE

DOCUMENTATION  
ONLINE  
[www.microchip.com](http://www.microchip.com)

## ALL SYSTEMS GO

- ✓ AUTOMOTIVE CONTROL
- ✓ TELECOMMUNICATIONS
- ✓ CONSUMER
- ✓ OFFICE AUTOMATION/EDP
- ✓ INDUSTRIAL CONTROL
- ✓ MECHATRONICS
- ✓ SECURITY

### PRICE GAUGE



### GLOBAL DISTRIBUTION



SERVICE & SUPPORT



### PERIPHERALS

ANALOG TIMERS  
PWM I2C  
USART CAN

### LEAD TIME



**MPLAB™ ICE 2000**  
EMULATION IN PROGRESS

ACCESS CONTROL

**K** SECURITY  
ARMED



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