

PIC24FJ128GA010 Family Rev. A3 Silicon Errata

The PIC24FJ128GA010 Family Rev. A3 parts you have received conform functionally to the Device Data Sheet (DS39747C), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC24FJ128GA010 Family will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC24FJ128GA010 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC24FJ128GA010	040Dh	03h
PIC24FJ96GA010	040Ch	03h
PIC24FJ64GA010	040Bh	03h
PIC24FJ128GA008	040Ah	03h
PIC24FJ96GA008	0409h	03h
PIC24FJ64GA008	0408h	03h
PIC24FJ128GA006	0407h	03h
PIC24FJ96GA006	0406h	03h
PIC24FJ64GA006	0405h	03h

The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory. They are shown in hexadecimal in the format "DEVID DEVREV".

1. Module: Core

With Doze mode enabled, DOZEN (CLKDIV<11>) set, and the CPU Peripheral Clock Ratio Select bits (CLKDIV<14:12>) configured to any value except 0b000, writes to SFR locations can not be performed.

Work around

Disable Doze mode, or select 1:1 CPU peripheral clock ratio before modifying stated SFR locations, or avoid writing stated locations while Doze mode is enabled and CPU peripheral clock ratio other than 1:1 is selected. Configure the device prior to entering Doze mode and use the mode only to monitor applications activity.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: JTAG

The current JTAG programming implementation is not compatible with third party programmers using SVF (Serial Vector Format) description language. JTAG boundary scan is supported by third party JTAG solutions and is not affected.

Work around

JTAG programming can be accomplished using custom JTAG software. The current implementation may not be supported in future PIC24F revisions.

Date Codes that pertain to this issue:

All engineering and production devices.

3 Module: PMP

In Master mode (MODE<1:0> = 11 or 10), back-to-back operations may cause the PMRD signal to not be generated. This limitation occurs when the peripheral is configured for zero wait states (WAITM<3:0> = 0000).

Work around

The PMRD signal will be generated correctly if a minimum of one instruction cycle delay is inserted between the back-to-back operations. A NOP instruction, or any other instruction, is adequate. Selecting a delay other than zero will also permit the PMRD signal to be generated.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Interrupts

The device may not exit Doze mode if certain trap conditions occur. Address error, stack error and math error traps are affected. Oscillator failure and all interrupt sources are not affected and can cause the device to correctly exit Doze mode.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

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5. Module: Output Compare

The output compare module may output a single glitch for one T_{CY} after the module is enabled ($OCM<2:0> = 000$). This issue occurs when the output state of the associated Data Latch register ($LATx$) is in the opposite state of the Output Compare mode when the peripheral is enabled. It can also occur when switching between two Output Compare modes with opposite output states.

Work around

If the output glitch must be avoided, verify that the associated data latch value of the OCx pin matches the initial state of the desired Output Compare mode. For example, if Output Compare 5 is configured for mode, $OCM<2:0> = 001$, ensure that the $LATD<4>$ bit is clear prior to writing the OCM bits. The port latch output value will match the initial output state of the $OC5$ pin and avoid the glitch when the peripheral is enabled.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: UART

The timing for transmitting a Sync Break has changed for this revision of silicon. The Sync Break is transmitted as soon as the $UTXBRK$ bit is set. A dummy write to $UxTXREG$ is still required and must be performed before the Sync Break has finished transmitting. Otherwise, the $UxTX$ may be held in the active state until the write has occurred.

Work around

Set the $UTXBRK$ bit when a Sync Break is required and perform a dummy $UxTXREG$ immediately following. This sequence will avoid holding the $UxTX$ pin in the active state.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: UART

UART receptions may be corrupted if the Baud Rate Generator (BRG) is set up for 4x mode ($BRGH = 1$) and an odd value is loaded in the Baud Rate Generator Prescaler register ($UxBRG$). Transmissions are not affected.

Work around

Use the 16x baud rate option ($BRGH = 0$) and adjust the baud rate accordingly.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: UART

UART1 and UART2 hardware flow control options are not available for the 64-pin variants of the PIC24FJ128GA010 product family. As a result, the $UxCTS$ and $UxRTS$ pins not available and the $UEN<1:0>$ control bits are read as '0' (unimplemented). UART2 hardware flow control is not available for the 80-pin PIC24FJ128GA010 variants. Therefore associated pins and bits are not available for these devices.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: UART

The auto-baud feature may not calculate the correct baud rate when the High Baud Rate Enable bit, BRG , is set. With the BRG set, the baud rate calculation used is the same as $BRG = 0$.

Work around

If the auto-baud feature is needed, use the Low Baud Rate mode by clearing the BRG bit.

10. Module: UART

With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.

Work around

To prevent the Sync Break character from being loaded into the FIFO, load the $UxBRG$ register with either 0x0000 or 0xFFFF prior to enabling the auto-baud feature ($ABAUD = 1$).

11. Module: A/D

Gain error may be as high as 5 LSbs for external references ($VREF+$ and $VREF-$) and 6 LSbs for internal reference ($AVDD$ and $AVSS$).

Work around

Determine gain error from a known reference voltage and compensate the A/D result in software.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: A/D

With the External Interrupt 0 (INT0) selected to start an A/D conversion (SSRC<2:0> = 001), the device may not wake-up from Sleep or Idle mode if more than one conversion is selected per interrupt (SMPI<3:0> <> 0000). Interrupts are generated correctly if the device is not in a Sleep or Idle mode.

Work around

Configure the A/D to generate an interrupt after every conversion (SMPI<3:0> = 0000). Use another wake-up source, such as the WDT or another interrupt source, to exit the Sleep or Idle mode. Alternatively, perform A/D conversions in Run mode.

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: SPI

The Enhanced SPI modes, selected by setting the Enhanced Buffer Enable bit, SPIBEN (SPIxCON2<0>), are not available.

Work around

Use Standard SPI mode by clearing the SPI Enhanced Buffer Enable bit, SPIBEN.

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: SPI

Master mode receptions using the SPI1 and SPI2 modules may not function correctly for bit rates above 8 Mbps if the master has the SMP bit (SPIxCON1<9>) cleared (master samples data at the middle of the serial clock period).

In this case, the data transmitted by the slave is received, shifted right by one bit, by the master. For example, if the data transmitted by the slave was 0xAAAA, the data received by the master would be 0x5555 (0xAAAA shifted right by one bit).

Work around

Users may set up the SPI module so that the bit rate is 8 Mbps or lower.

Alternatively, the bit rate can be configured higher than 8 Mbps, but the SMP bit (SPIxCON1<9>) of the SPI master must be set (master samples data at the end of the serial clock period).

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: SPI

A frame synchronization pulse may not be output in SPI Master mode if the pulse is selected to coincide with the first bit clock (SPIFE = 1). SCKx and SDOx waveforms are not affected.

Work around

Select the frame synchronization pulses to proceed the first bit clock (SPIFE = 0). The frame pulses will output correctly as described in the product data sheet.

Date Codes that pertain to this issue:

All engineering and production devices.

16. Module: SPI

In SPI Slave mode (MSTEN = 0), with the slave select option enabled (SSEN = 1), the peripheral may accept transfers regardless of the SSx pin state. The received data in SSPxBUF will be accurate but not intended for the device.

Work around

If the Slave select option is required (e.g., device one of multiple SPI slave nodes on an SPI network), two potential work arounds exist:

1. Configure the port associated with SSx to an input and periodically read the PORT register. If the pin is read '0', disable the SPI peripheral (SPIEN = 0). Enable the peripheral (SPIEN = 1) if the pin is read as a logic '1'.
2. Read the pin associated with SSx after a transfer is complete, indicated by the SPIxF bit being set. If the port pin is read as a digital '1', read SSPxBUF and discard the contents.

Date Codes that pertain to this issue:

All engineering and production devices.

17. Module: Oscillator

The Two-Speed Start-up feature may not be available on exit from Sleep mode with the IESO (Internal/External Switchover mode) enabled. Upon wake-up, the device will wait for the clock source used prior to entering Sleep mode to become ready.

Work around

None.

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REVISION HISTORY

Rev A Document (11/2006)

First revision of this document. Includes silicon issues 1 (Core), 2 (JTAG), 3 (PMP), 4 (Interrupts), 5 (Output Compare), 6-10 (UART), 11-12 (A/D), 13-16 (SPI) and 17 (Oscillator).

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